HYPPI: THE NEW PATH OF MOORE'S LAW IN CLEAR LIGHT

Shuai Sun, Vikram Narayana, Tarek El-Ghazawi, Volker J. Sorger

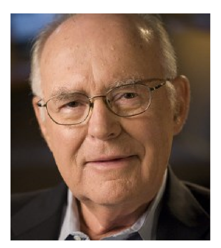
Department of Electrical and Computer Engineering, The George Washington University

AFOSR AIR FORCE OFFICE OF SCIENTIFIC RESEARCH

THE GEORGE WASHINGTON UNIVERSITY

Motivation

As the observed pace of the semiconductor industry notably slowing down especially since the **14 nm technology node**, the electronics is suffering from the physical limits of scaling more than ever before.



"Transistors double every 12 months."

— *Gordon Moore*

"Transistors get smaller; power density stays constant."

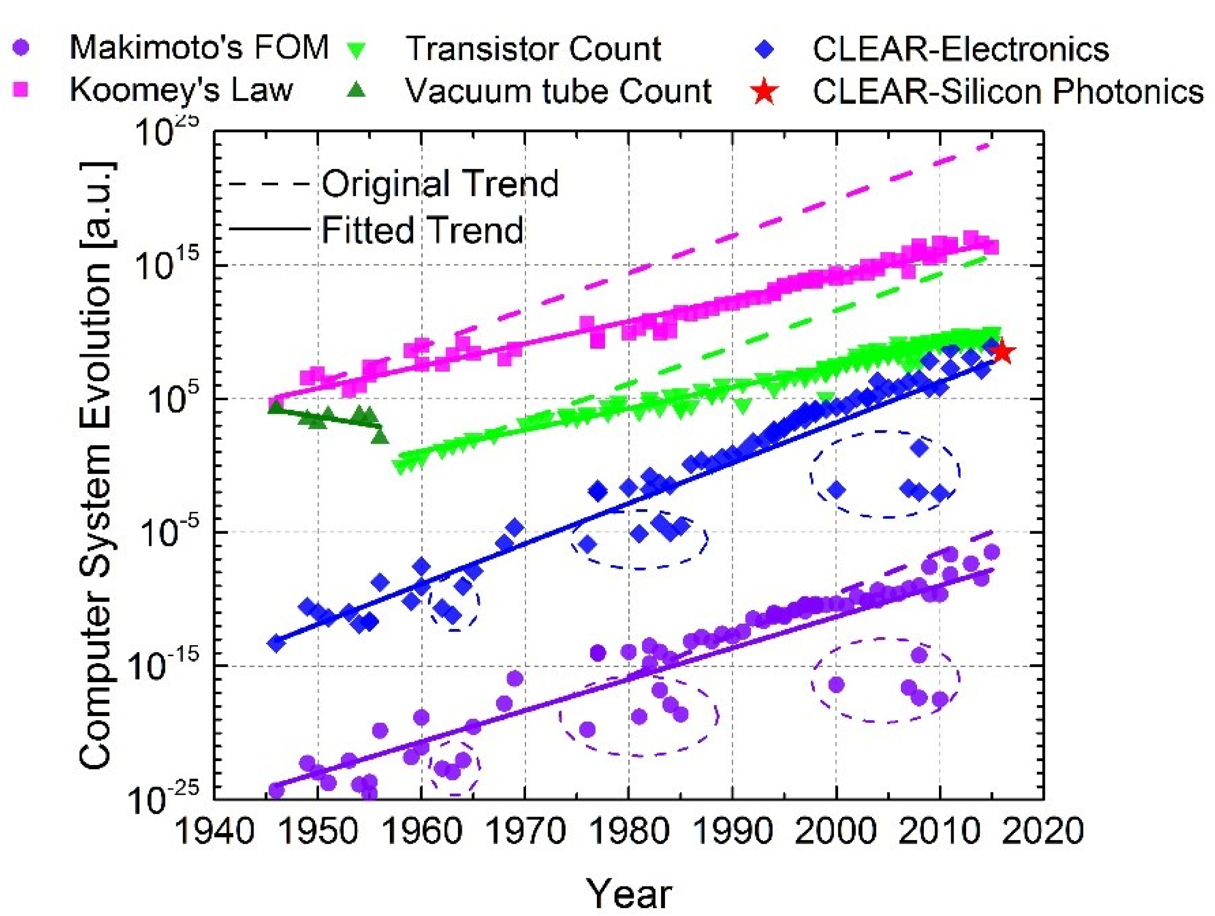
— *Robert Dennard*

"The computation efficiency doubles every 1.57 years."

— *Jonathan Koomey*

With rapidly rising machine performance the communicate–to-compute overhead is increasing, making a case to use silicon photonics and possibly plasmonics on-chip while mitigating challenges in:

- the increasing **power density**
- strict **heat budget**
- higher **data bandwidth** requirement

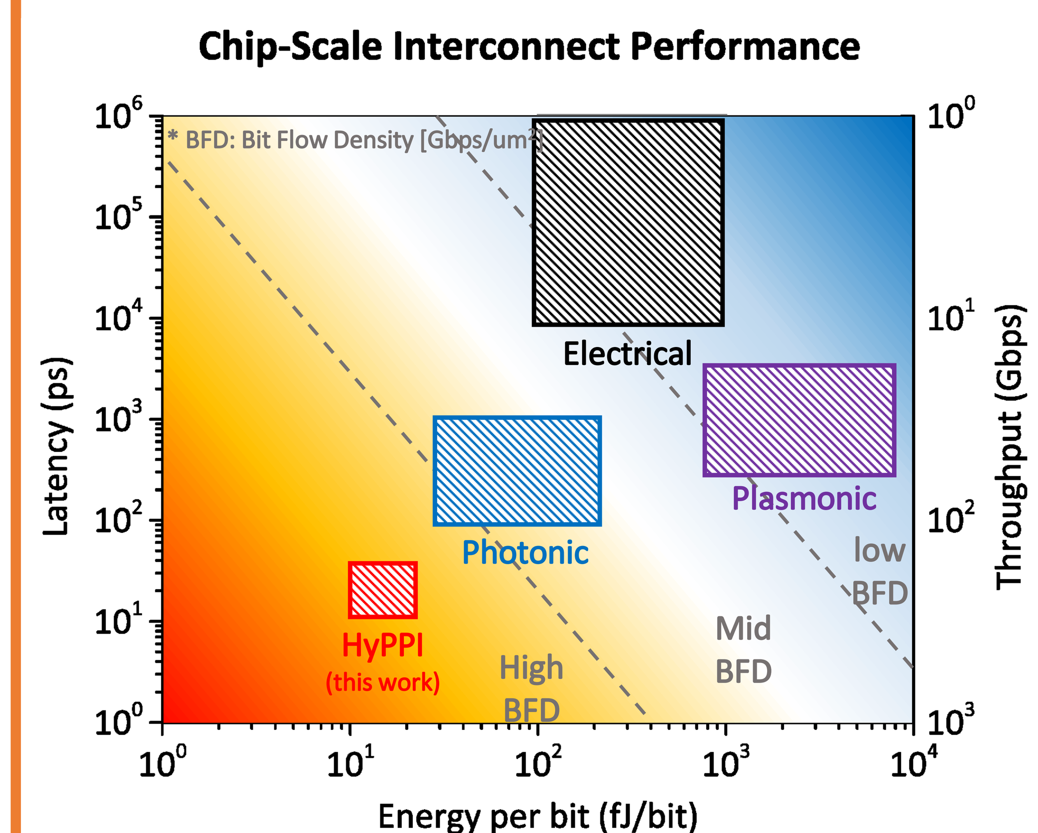


$$\text{CLEAR} = \frac{\text{Capability}}{\text{Latency} \times \text{Energy} \times \text{Amount} \times \text{Resistance}}$$

This universal metric termed **Capability to Latency Energy Amount Resistance** (CLEAR) is:

- a holistic set of performance parameters cover both physical and economic factors
- able to post- and predict a constant evolution rate of compute system
- valid among different technology cycles

Abstract



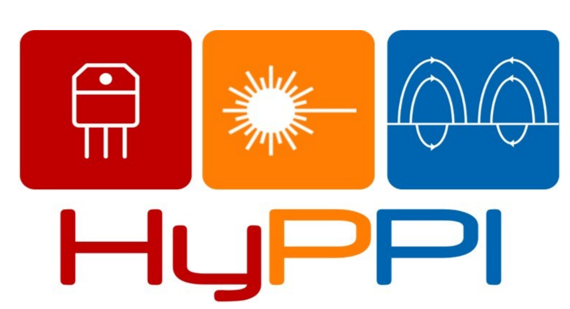
In this project, we proposed the first holistic figure of merit termed **Capability to Latency Energy Amount Resistance (CLEAR)** to accurately evaluate compute system evolution. Driven from both physical and economic factors, CLEAR can also be applied for device, link and network comparison among various technology options, such as electronics, photonics, plasmonics and **hybrid photonic plasmonics (HyPPI)**. The project will follow the steps below:

- A holistic metric CLEAR for performance-cost evaluation
- Novel technology HyPPI with superior performance
- CLEAR evaluation at device and link levels
- Configurable HyPPI using CLEAR for dynamically control

Technology Comparison

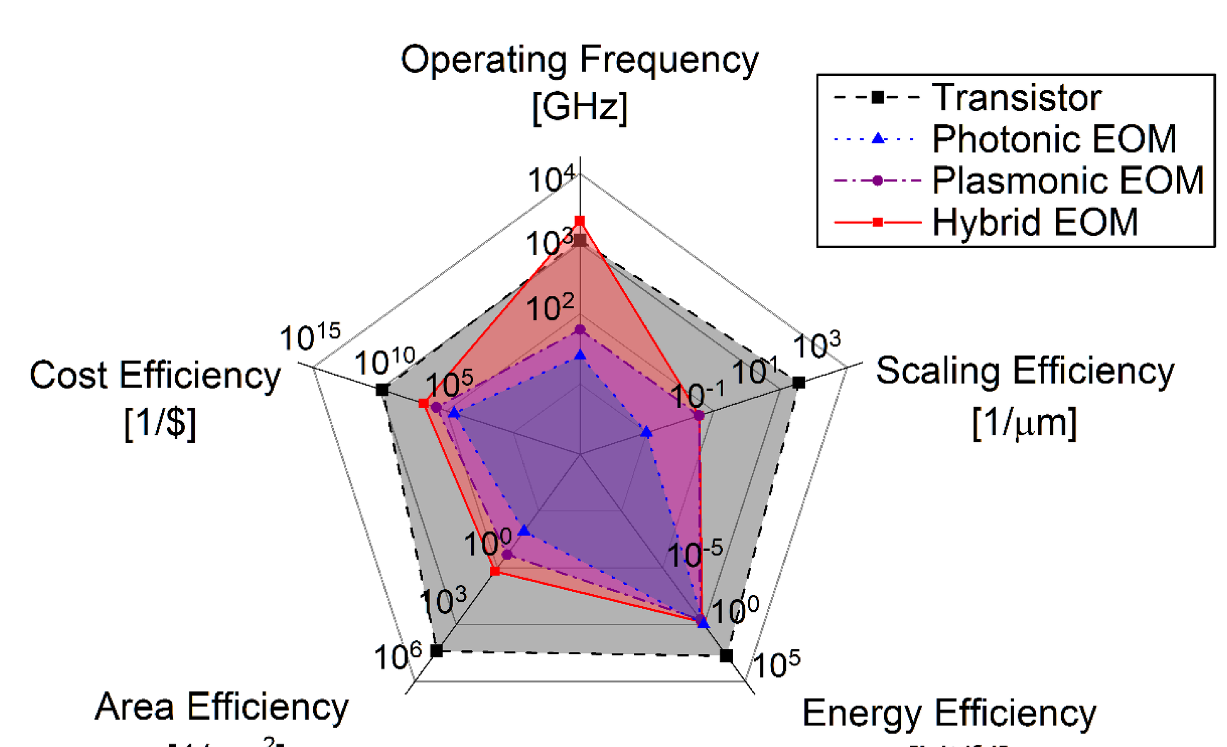
The **hybrid photonic plasmonic interconnect** (HyPPI) combines both low loss photonic signal routing and the ultra-compact plasmonic devices.

Photonics	Plasmonics
☒ Diffraction Limited	☑ No Diffraction Limit
☒ Large Footprint	☑ Area Efficient
☒ Low LMI	☑ Energy Efficient
☑ Long Propagation	☒ Short Propagation



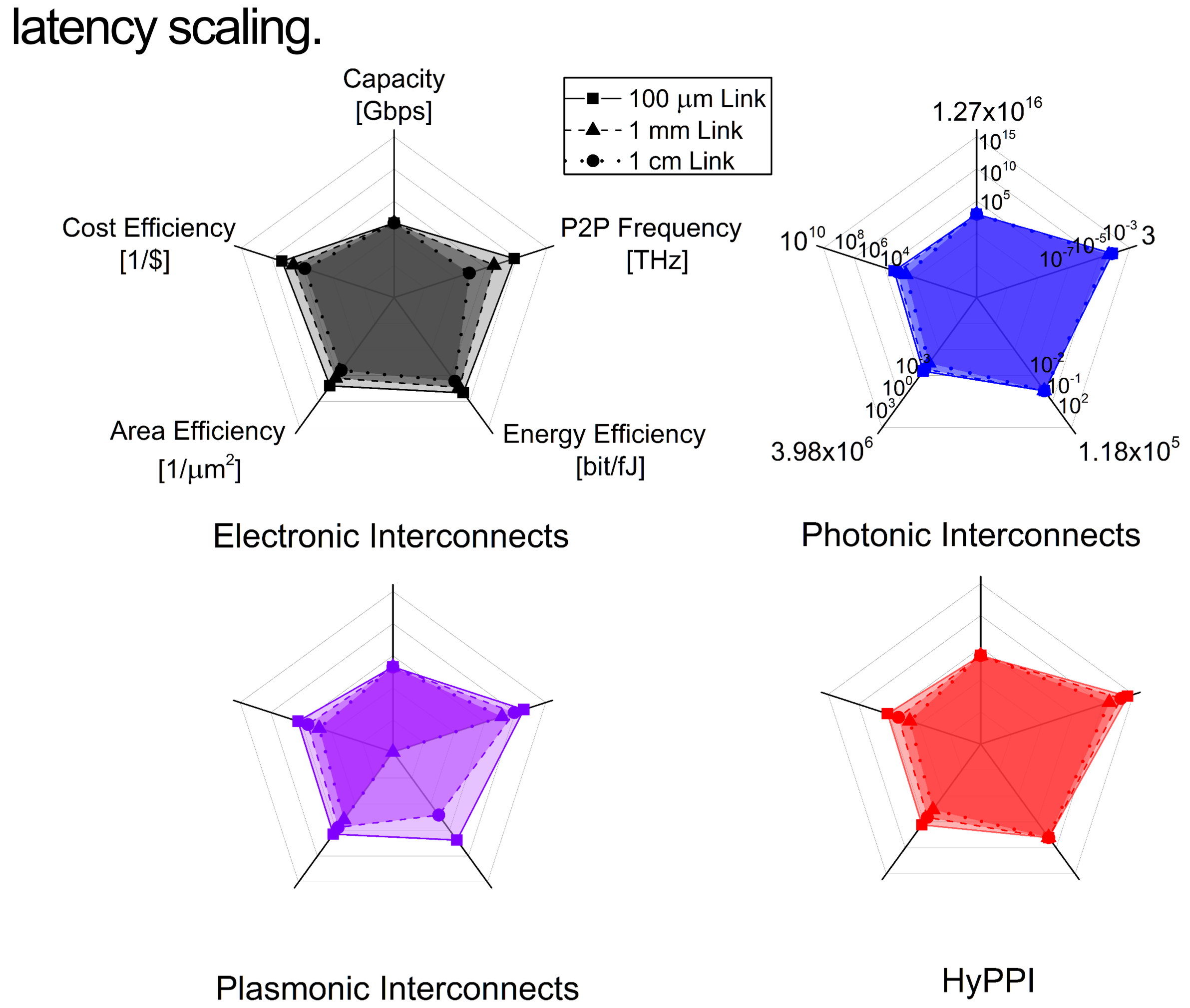
CLEAR at Device Level

Each axis represents one factor of the device-CLEAR and is scaled to the **actual physical limit** of each factor. The colored area of each device also demonstrates the CLEAR value of each device.

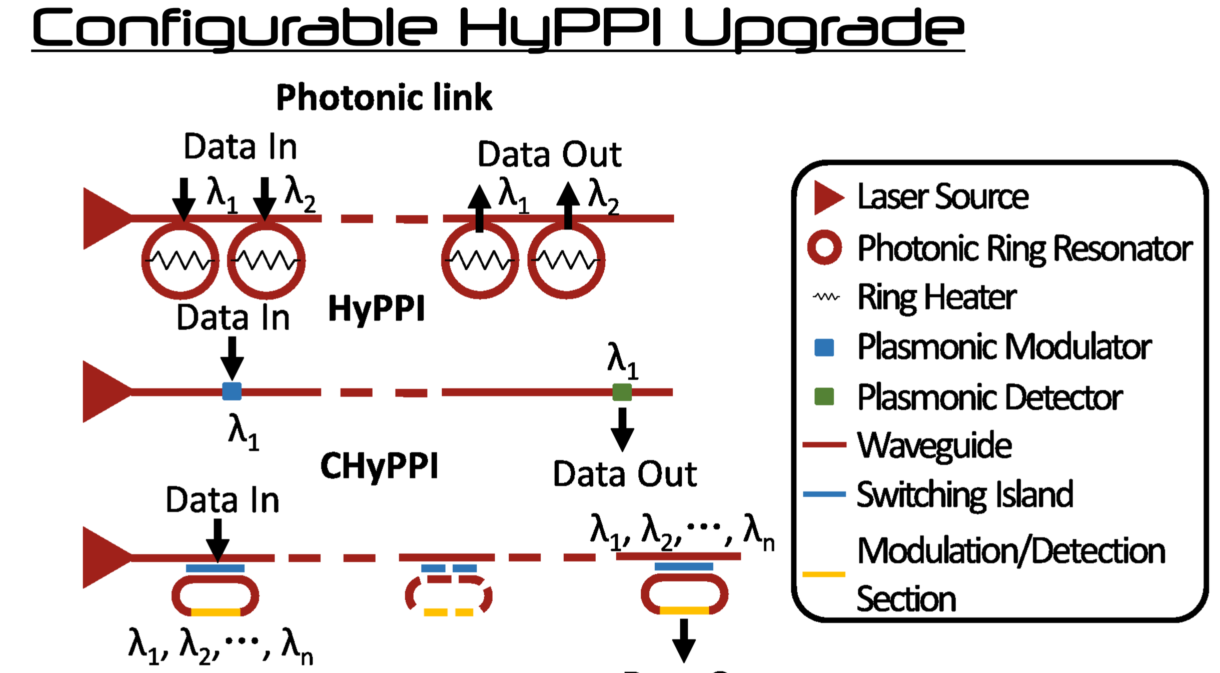


CLEAR at Link Level

All four link-CLEAR at **100 μm, 1mm and 1cm** distance are scaled by the physical limit. In general, all four link options have significant room for further development while optical links have greater potentials in the energy efficiency and latency scaling.

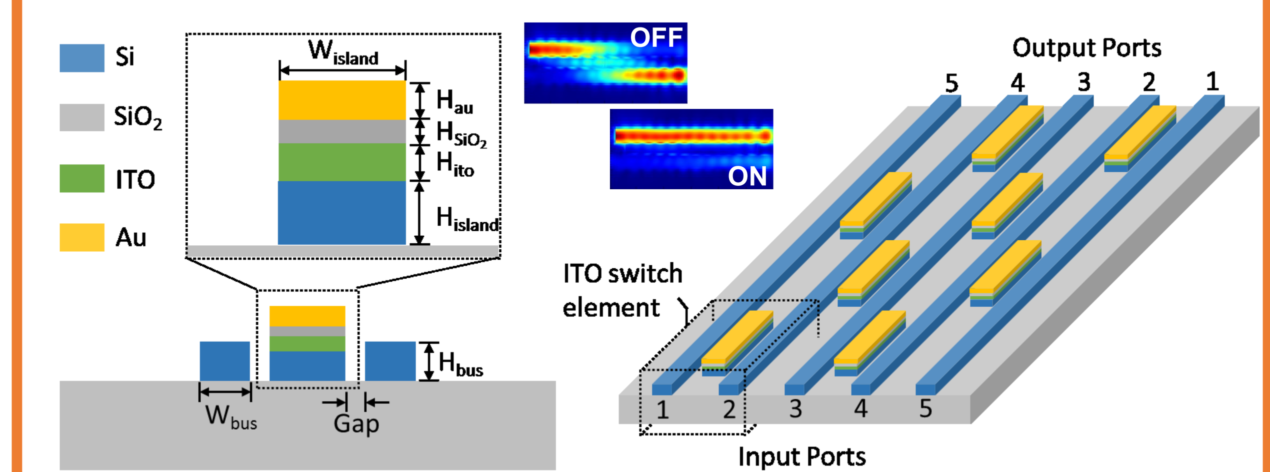


Configurable HyPPI Upgrade



Smart HyPPI

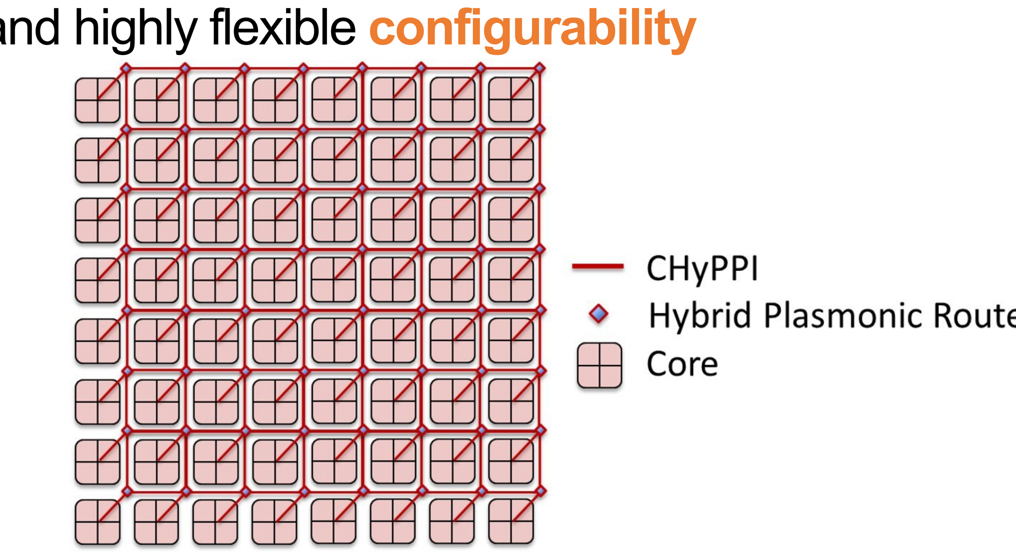
Hybrid Plasmonic Router



CHyPPI with **machine learning module** could give the optical NoC higher performance depending on different applications with various data traffic pattern by using CLEAR as the holistic metric of the network.

As traditional nanophotonics options face limitations such as **higher static power** and the **low operating frequency** due to large device capacitances, CHyPPI integrated with electro-optic NoC (256-core network) is able to achieve:

- superior energy efficiency with **3.5 Watt** static power
- **7 mm²** on-chip area cost
- and highly flexible **configurability**



Our Work

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